

Attorney's Docket No.:10559-389001/P10252

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method comprising:
detecting a reset condition;
verifying a memory controller is initialized by
determining if a reset signal is detected for a predetermined
period of time; and
placing a memory system into a self-refresh mode using
a state machine in the memory controller.
2. (Original) The method of Claim 1, further
comprising verifying the memory controller is initialized by
delaying a reset signal.
3. (Original) The method of Claim 1, further
comprising monitoring the voltage level of a system to determine
a power failure.
4. (Original) The method of Claim 3, further
comprising generating a reset condition when either a power
failure or a reset request occurs.
5. (Original) The method of Claim 4, further
comprising verifying the reset request does not occur prior to
initialization.
6. (Original) The method of Claim 1, further
comprising detecting the reset condition and verifying the
memory controller is initialized external to the memory
controller.

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7-12. (Canceled)

13. (Currently Amended) The method of claim 1, wherein the detecting a reset condition ~~A method placing a memory system in a data self-refresh mode comprising:~~

detects ~~detecting~~ either a power failure or reset signal; and

further comprises:

generating a delay signal based on the reset signal; and

initiating a self-refresh routine if the delay signal indicates the memory system is initialized.

14. (Original) The method of Claim 13 further comprising monitoring the voltage level of a system to determine a power failure.

15. (Currently Amended) The method of Claim 13, further comprising generating two output signals by the power fail controller to the state machine ~~to the memory controller~~ based on the reset signal.

16. (Previously presented) The method of claim 13, further comprising preventing initiating the self-refresh routine if the reset signal is not asserted for a predetermined period of time.

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17. (New) A system comprising:

a voltage monitor to monitor a voltage of the system and to transmit a voltage monitor signal if the voltage falls below a predetermined threshold;

a power delay circuit to transmit a power delay signal in response to receiving a voltage monitor signal and to transmit a reset signal if the voltage monitor signal indicates a reset condition or in response to an external event reset signal;

a memory sub-system to store digital data and having a self-refresh circuit, the self-refresh circuit causing the memory sub-system to enter into a self-refresh sequence; and

a memory controller to control and configure the memory sub-system, the memory controller having a power fail controller to receive a power delay signal or a reset signal from the power delay circuit, the power controller asserting a system reset signal and sending two configuration signals in response to the power delay signal or external event reset signal, the configuration signals indicating whether the external event reset signal was detected for at least a predetermined amount of time and at least one of a power failure or an external reset event is detected.

18. (New) The system of claim 17, wherein the memory controller further comprises a state machine to receive the system reset signal and the configuration signals and to direct the memory sub-system into a self-refresh state based on the system reset signal and the configuration signals.

19. (New) The system of claim 17, further comprising means for generating an external event signal.

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20. (New) The system of claim 17, wherein the power fail controller prevents the self-refresh sequence from executing when the system is not configured.

21. (New) A method comprising:
monitoring a voltage of a system;
transmitting a voltage monitor signal if the voltage falls below a predetermined threshold;
transmitting a power delay signal in response to the voltage monitor signal;
transmitting a reset signal if the voltage monitor signal indicates a reset condition or in response to an external event reset signal; and
asserting a system reset signal and sending two configuration signals in response to the power delay signal or reset signal, the configuration signals indicating whether the external event reset signal was detected for at least a predetermined amount of time and at least one of a power failure or an external reset event is detected.